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S2	10609	\$3selected adj wordline or \$3selected adj word adj line	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/12 15:03
S3	709	\$3selected adj wordline with negative or \$3selected adj word adj line with negative	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/12 15:03
S4	161	S3 and decoder near5 negative	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/12 15:04
S5	1175785	S4 and negative and voltage or potential	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/12 15:04
S6	161	S4 and negative and (voltage or potential)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/12 15:05
S7	97	S6 and decoder with negative with \$3selected	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/12 15:05
S8	73	S7 and positive with selected with S1	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/12 15:06

S9	68	S8 and "365"/\$.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/12 15:16
S10	2	"6058060".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/12 15:17

US-PAT-NO:	5622222	LAST Advanced find			
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Abstract Text - ABTX (1):

There is provided a nonvolatile semiconductor memory which can simplify a circuit structure of a row decoder circuit to minimize an increase in chip size, and selectively supply a negative voltage to a word line. The nonvolatile semiconductor memory has a row decoder circuit section for selecting one of word lines in a memory cell array in response to an input address, and outputting a negative voltage or high voltage to the selected word line in accordance with a selected mode while outputting a ground potential to non-selected word lines. In such a nonvolatile semiconductor memory, each of predecoders comprises supply voltage-high voltage and ground-negative voltage converting circuits for converting the output levels into levels of supply voltage-high voltage and ground-negative voltage respectively in response to the input address, high voltage and negative voltage drivers for outputting from the first and second terminals the high voltage or the negative voltage in accordance with each output from these converting circuits, and a select address driver for outputting a voltage activated by the outputs of the voltage drivers and switched by the selected mode.

Brief Summary Text - BSTX (3):

The present invention relates to a nonvolatile semiconductor memory, and in particular, to a negative-voltage row-decoder circuit in a flash EEPROM (Electrically Erasable/Programmable Read Only Memory).

Brief Summary Text - BSTX (5):

When writing or erasing data into or from a flash EEPROM with memory cells each having a floating gate, application of a negative voltage to a gate of a memory transistor is a very important technique in attaining low voltage and high reliability of the device. If the writing or erasing of data is done in a small unit of capacity, a row decoder circuit to supply only a selected word line with a negative or high voltage is required.

Brief Summary Text - BSTX (6):

Now, description is made as to memory cells in such a flash EEPROM. Table 1 shows exemplary conditions of bias voltage applied to respective terminals of a memory cell when erase and write operations are performed by using Fowler-Nordheim tunnel current. FIGS. 1A and 1B are schematic sectional views of the memory cell in the respective operations. In read-out operation, a control gate 31 is supplied with 5.0 V., a drain 33 with 1.0 V. and a source 32

U.S. Patent Oct. 26, 1999 Sheet 2 of 10 5,973,963

Oct. 26, 194

Sheet 2 of 10

5,973,963

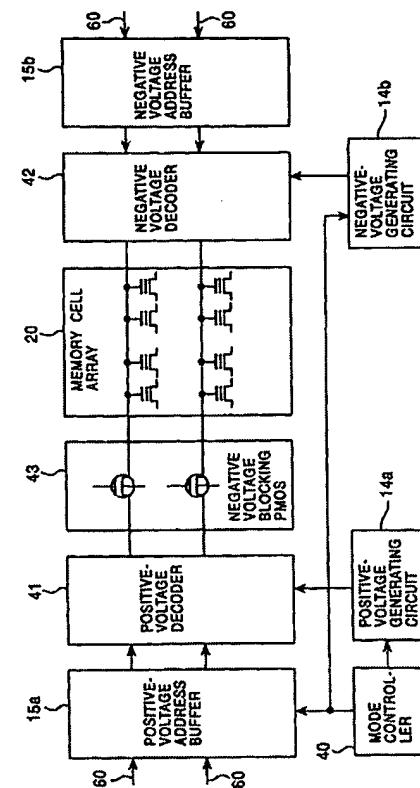


FIG. 2 (PRIOR ART)

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@PJL SET JOBATTR="JobAcct2=WS08

US-PAT-NO: 6097665 EAST Advanced Text

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TITLE: Dyna charge

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Abstract Text - ABTX (1):

Level converter converts a word line group specifying signal, which is sent from a row decoder and has amplitude of a power supply potential V_{CC} and a ground potential GND , into mutually complementary logic signals WD and ZWD of a high voltage V_{PP} and a negative potential V_{BB} . An RX decoder decodes an address signal to output a signal of an amplitude of $(V_{PP}-V_{BB})$ specifying a word line in a word line group. A word driver provided corresponding to each word line transmits a word line specifying signal or a negative potential to the corresponding word line in accordance with signals WD and ZWD sent from a level converting circuit. The nonselected word line receives negative potential V_{BB} from a word driver. The selected word line receives high voltage V_{PP} from the word driver. It is possible to suppress a channel leak current at a memory transistor in the nonselected memory cell, which may be caused by the potential change of the word line and/or bit line, and a charge holding characteristic of the memory cell can be improved.

Brief Summary Text - BSTX (5):

FIG. 63 schematically shows a whole structure of a dynamic semiconductor memory device (will be referred to as "DRAM") in the prior art. In FIG. 63, the DRAM includes a memory cell array 900 having memory cells MC arranged in a matrix of rows and columns. In memory cell array 900, a word line WL is provided corresponding to each row of memory cells MC, and a column line (bit line pair BL and $/BL$) is provided corresponding to each column of memory cells MC. FIG. 63 representatively shows one word line WL and one bit line pair BL and $/BL$. Memory cell MC is provided corresponding to a crossing of bit line pair BL and $/BL$ and word line WL. In FIG. 63, memory cell MC is provided corresponding to the crossing of bit line BL and word line WL, as an example. Memory cell MC includes a capacitor MQ storing information in the form of electric charges, and a memory transistor MT which is responsive to a signal potential on word line WL to be turned on to connect memory capacitor MQ to bit line BL (or $/BL$).

Brief Summary Text - BSTX (6):

The DRAM further includes an address buffer 902 which produces an internal address signal from an externally applied address signal, a row decode circuit 904 which decodes the internal row address signal sent from address buffer 902 to produce a decode signal specifying a corresponding word line in memory cell

United States Patent 6,097,665
Tomishima et al.

(11) Patent Number: 6,097,665
(43) Date of Patent: Aug. 1, 2000

(54) DYNAMIC SEMICONDUCTOR MEMORY DEVICE HAVING EXCELLENT CHARGE RETENTION CHARACTERISTICS

FOREIGN PATENT DOCUMENTS

6-299965 10/1985 Japan

6-279265 01/1992 Japan

6-322065 07/1992 Japan

(75) Inventor: Shigeki Tomishima, Kanetoshi Arimoto, both of Kyoto, Japan

OTHER PUBLICATIONS

(73) Assignee: Mitsubishi Denki Kabushiki Kaisha, Tokyo, Japan

Y. Nakagawa et al., "High-1-V Series-Resistor Architecture for Power-Low-Power VLSI", 1992 Symposium on VLSI Circuits Digest of Technical Papers, pp. 52-53.

(21) Appl. No.: 09/181,562

Primary Examiner-A. Zarbini

(22) Filed: Oct. 29, 1998

Attorney, Agent, or Firm-McMahon, Will & Emery

Related U.S. Application Data

(57) ABSTRACT

(62) Division of application No. 08/790,230, Jan. 26, 1997, Pat. No. 5,870,740, which is a division of application No. 08/682,731, May 21, 1997, Pat. No. 5,811,961.

(36) Foreign Application Priority Data

May 11, 1994 [JP] Japan

(51) Int. Cl.7 D1C 8/00

(52) U.S. Cl. 345/230.04, 345/230.03

(44) Field of Search 345/230.05, 180.11, 345/149, 218, 230/03

(56) References Cited

U.S. PATENT DOCUMENTS

3,634,064 7/1972 Nagatsu -

4,315,309 2/1982 Ichijo -

4,628,386 12/1996 Saito -

4,853,659 1/1990 Nakano -

5,297,004 3/1994 Nakano -

5,522,323 2/1996 Amano et al. -

5,572,702 1/1997 Goto et al. -

5,621,910 4/1997 Nakano -

5,621,911 4/1997 Nakano -

5,621,912 4/1997 Nakano -

5,621,913 4/1997 Nakano -

5,621,914 4/1997 Nakano -

5,621,915 4/1997 Nakano -

5,621,916 4/1997 Nakano -

5,621,917 4/1997 Nakano -

5,621,918 4/1997 Nakano -

5,621,919 4/1997 Nakano -

5,621,920 4/1997 Nakano -

5,621,921 4/1997 Nakano -

5,621,922 4/1997 Nakano -

5,621,923 4/1997 Nakano -

5,621,924 4/1997 Nakano -

5,621,925 4/1997 Nakano -

5,621,926 4/1997 Nakano -

5,621,927 4/1997 Nakano -

5,621,928 4/1997 Nakano -

5,621,929 4/1997 Nakano -

5,621,930 4/1997 Nakano -

5,621,931 4/1997 Nakano -

5,621,932 4/1997 Nakano -

5,621,933 4/1997 Nakano -

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5,621,935 4/1997 Nakano -

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5,621,937 4/1997 Nakano -

5,621,938 4/1997 Nakano -

5,621,939 4/1997 Nakano -

5,621,940 4/1997 Nakano -

5,621,941 4/1997 Nakano -

5,621,942 4/1997 Nakano -

5,621,943 4/1997 Nakano -

5,621,944 4/1997 Nakano -

5,621,945 4/1997 Nakano -

5,621,946 4/1997 Nakano -

5,621,947 4/1997 Nakano -

5,621,948 4/1997 Nakano -

5,621,949 4/1997 Nakano -

5,621,950 4/1997 Nakano -

5,621,951 4/1997 Nakano -

5,621,952 4/1997 Nakano -

5,621,953 4/1997 Nakano -

5,621,954 4/1997 Nakano -

5,621,955 4/1997 Nakano -

5,621,956 4/1997 Nakano -

5,621,957 4/1997 Nakano -

5,621,958 4/1997 Nakano -

5,621,959 4/1997 Nakano -

5,621,960 4/1997 Nakano -

5,621,961 4/1997 Nakano -

5,621,962 4/1997 Nakano -

5,621,963 4/1997 Nakano -

5,621,964 4/1997 Nakano -

5,621,965 4/1997 Nakano -

5,621,966 4/1997 Nakano -

5,621,967 4/1997 Nakano -

5,621,968 4/1997 Nakano -

5,621,969 4/1997 Nakano -

5,621,970 4/1997 Nakano -

5,621,971 4/1997 Nakano -

5,621,972 4/1997 Nakano -

5,621,973 4/1997 Nakano -

5,621,974 4/1997 Nakano -

5,621,975 4/1997 Nakano -

5,621,976 4/1997 Nakano -

5,621,977 4/1997 Nakano -

5,621,978 4/1997 Nakano -

5,621,979 4/1997 Nakano -

5,621,980 4/1997 Nakano -

5,621,981 4/1997 Nakano -

5,621,982 4/1997 Nakano -

5,621,983 4/1997 Nakano -

5,621,984 4/1997 Nakano -

5,621,985 4/1997 Nakano -

5,621,986 4/1997 Nakano -

5,621,987 4/1997 Nakano -

5,621,988 4/1997 Nakano -

5,621,989 4/1997 Nakano -

5,621,990 4/1997 Nakano -

5,621,991 4/1997 Nakano -

5,621,992 4/1997 Nakano -

5,621,993 4/1997 Nakano -

5,621,994 4/1997 Nakano -

5,621,995 4/1997 Nakano -

5,621,996 4/1997 Nakano -

5,621,997 4/1997 Nakano -

5,621,998 4/1997 Nakano -

5,621,999 4/1997 Nakano -

5,621,990 4/1997 Nakano -

5,621,991 4/1997 Nakano -

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5,621,996 4/1997 Nakano -

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5,621,991 4/1997 Nakano -

5,621,992 4/1997 Nakano -

5,621,993 4/1997 Nakano -

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5,621,997 4/1997 Nakano -

5,621,998 4/1997 Nakano -

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5,621,990 4/1997 Nakano -

5,621,991 4/1997 Nakano -

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5,621,998 4/1997 Nakano -

5,621,999 4/1997 Nakano -

5,621,990 4/1997 Nakano -

5,621,991 4/1997 Nakano -

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5,621,994 4/1997 Nakano -

5,621,995 4/1997 Nakano -

5,621,996 4/1997 Nakano -

5,621,997 4/1997 Nakano -

5,621,998 4/1997 Nakano -

5,621,999 4/1997 Nakano -

5,621,990 4/1997 Nakano -

5,621,991 4/1997 Nakano -

5,621,992 4/1997 Nakano -

5,621,993 4/1997 Nakano -

5,621,994 4/1997 Nakano -

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5,621,996 4/1997 Nakano -

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Abstract Text - ABTX (1):
 Level converter converts a word line group specifying signal, which is sent from a row decoder and has amplitude of a power supply potential V_{CC} and a ground potential GND , into mutually complementary logic signals WD and ZWD of a high voltage V_{PP} and a negative potential V_{BB} . An RX decoder decodes an address signal to output a signal of an amplitude of $(V_{PP}-V_{BB})$ specifying a word line in a word line group. A word driver provided corresponding to each word line transmits a word line specifying signal or a negative potential to the corresponding word line in accordance with signals WD and ZWD sent from a level converting circuit. The nonselected word line receives negative potential V_{BB} from a word driver. The selected word line receives high voltage V_{PP} from the word driver. It is possible to suppress a channel leak current at a memory transistor in the nonselected memory cell, which may be caused by the potential change of the word line and/or bit line, and a charge holding characteristic of the memory cell can be improved.

Brief Summary Text - BSTX (5):
 FIG. 63 schematically shows a whole structure of a dynamic semiconductor memory device (will be referred to as "DRAM") in the prior art. In FIG. 63, the DRAM includes a memory cell array 900 having memory cells MC arranged in a matrix of rows and columns. In memory cell array 900, a word line WL is provided corresponding to each row of memory cells MC, and a column line (bit line pair BL and $/BL$) is provided corresponding to each column of memory cells MC. FIG. 63 representatively shows one word line WL and one bit line pair BL and $/BL$. Memory cell MC is provided corresponding to a crossing of bit line pair BL and $/BL$ and word line WL. In FIG. 63, memory cell MC is provided corresponding to the crossing of bit line BL and word line WL, as an example. Memory cell MC includes a capacitor MQ storing information in the form of electric charges, and a memory transistor MT which is responsive to a signal potential on word line WL to be turned on to connect memory capacitor MQ to bit line BL (or $/BL$).

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 The DRAM further includes an address buffer 902 which produces an internal address signal from an externally applied address signal, a row decode circuit 904 which decodes the internal row address signal sent from address buffer 902 to produce a decode signal specifying a corresponding word line in memory cell

(12) United States Patent
 Tomishima et al.

(10) Patent No.: US 6,377,508 B1
 (11) Date of Patent: *Apr. 23, 2002

(54) DYNAMIC SEMICONDUCTOR MEMORY DEVICE HAVING EXCELLENT CHARGE RETENTION CHARACTERISTICS

5,321,350 A 3,994 Tomishima
 5,375,301 A 3,995 Tomishima
 5,382,213 A 3,995 Amano et al.
 5,337,362 A 7,149,038 Goto et al.

(75) Inventor: Shigeki Tomishima, Kazutomi Amano, both of Hyogo (JP)

JP 6,209,986 10,295
 JP 6,276,285 10,192
 JP 6,312,946 10,192

(13) Assignee: Mitsubishi Denki Kabushiki Kaisha, Tokyo (JP)

(15) Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/467,716

(22) Filed: Dec. 21, 1999

Related U.S. Application Data

(60) Continuation of application No. 09/181,642, filed on Oct. 20, 1998, which is a division of application No. 08/999,249, filed on Jan. 28, 1997, and Pat. No. 5,870,248, which is a division of application No. 08/485,748, filed on May 10, 1995, and Pat. No. 5,817,304.

(30) Foreign Application Priority Data

May 11, 1994 (JP) 6,097,511

(51) Int. Cl. 7 G11C 8/00
 (52) U.S. Cl. 365/230.06; 365/180.11
 (58) Field of Search 365/230.06, 365/11, 365/149, 218

References Cited

U.S. PATENT DOCUMENTS

3,824,364 A 7/1974 Wegener
 4,113,394 A 4/1978 Tolka
 4,638,260 A 12/1986 Kato

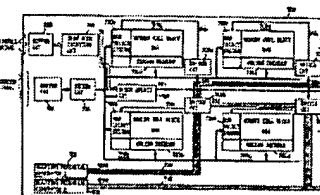
FOREIGN PATENT DOCUMENTS

"Sub-1-V Swing Bias Architecture for Future Low-Power DRAM", by Y. Nakajima et al., 1992 Symposium on VLSI Circuits Digest of Technical Papers, pp. 82-83.

OTHER PUBLICATIONS

Priority Examination--A. Zarabia
 (70) Attorney, Agent, or Firm--McMahon, Will & Emery
 (71) ABSTRACT
 Level converter converts a word line group specifying signal, which is sent from a row decoder and has amplitude of a power supply potential V_{CC} and a ground potential GND , into mutually complementary logic signals WD and ZWD of a high voltage V_{PP} and a negative potential V_{BB} . An RX decoder decodes an address signal to output a signal of an amplitude of $(V_{PP}-V_{BB})$ specifying a word line in a word line group. A word driver provided corresponding to each word line transmits a word line specifying signal or a negative potential to the corresponding word line in accordance with signals WD and ZWD sent from a level converting circuit. The nonselected word line receives negative potential V_{BB} from a word driver. The selected word line receives high voltage V_{PP} from the word driver. It is possible to suppress a channel leak current at a memory transistor in the nonselected memory cell, which may be caused by the potential change of the word line and/or bit line, and a charge holding characteristic of the memory cell can be improved.

45 Claims, 43 Drawing Sheets



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Level converter converts a word line group specifying signal, which is sent from a row decoder and has amplitude of a power supply potential Vcc and a ground potential GND, into mutually complementary logic signals WD and ZWD of a high voltage Vpp and a negative potential Vbb. An RX decoder decodes an address signal to output a signal of an amplitude of (Vpp-Vbb) specifying a word line in a word line group. A word driver provided corresponding to each word line transmits a word line specifying signal or a negative potential to the corresponding word line in accordance with signals WD and ZWD sent from a level converting circuit. The nonselected word line receives negative potential Vbb from a word driver. The selected word line receives high voltage Vpp from the word driver. It is possible to suppress a channel leak current at a memory transistor in the nonselected memory cell, which may be caused by the potential change of the word line and/or bit line, and a charge holding characteristic of the memory cell can be improved.

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United States Patent 1991 Patent Number: 5,870,348
Tomishima et al. Date of Patent: Feb. 9, 1999
US01870348A1

[54] DYNAMIC SEMICONDUCTOR MEMORY DEVICE HAVING BACK-END CHARGE RETENTION CHARACTERISTICS

[75] Inventor: Shigeki Tomishima, Kanetoshi Arimoto, both of Hyogo, Japan

[73] Assignee: Mitsubishi Denki Kabushiki Kaisha, Tokyo, Japan

[21] Appl. No.: 709,249
[22] Filed: Jan. 28, 1997

[62] Division of Ser. No. 436,766, May 16, 1995, Pat. No. 5,617,360.

[30] Foreign Application Priority Data
May 11, 1994 [JP] Japan 6-07211

[51] Int. Cl. 7 G11C 8/00
[52] U.S. Cl. 365/230.06, 365/199.11; 365/115

[38] Field of Search 365/230.06, 149, 365/199.11, 159.09, 214

[56] References Cited
U.S. PATENT DOCUMENTS

3,824,584 2,721 Weigert 3,651,011
4,211,299 2,722 Weigert 3,651,012
4,324,186 2,741,466 Saito 3,651,013
3,805,486 2,741,468 Hata 3,651,018
3,297,104 3,109,044 Nakashima 3,651,019
3,292,333 2,719,956 Arai 3,651,020
3,337,832 3,199,946 Gali 3,651,026

FOREIGN PATENT DOCUMENTS
60-29990 10/1985 Japan
61-77205 03/1986 Japan
61-19425 03/1986 Japan
61-32286 03/1992 Japan

OTHER PUBLICATIONS
"SBD-1-V SWING BUS ARCHITECTURE FOR FUTURE LOW-POWER ULSI", Nakagawa et al., 1992 Symposium on VLSI Circuits Digest of Technical Papers, pp. 32-43.

Primary Examiner—A. Zuchlis
Attorney, Agent, or Firm—McKenna, Will & Emery

(57) ABSTRACT
Level converter converts a word line group specifying signal, which is sent from a row decoder and has amplitude of a power supply potential Vcc and a ground potential GND, into mutually complementary logic signals WD and ZWD of a high voltage Vpp and a negative potential Vbb. An RX decoder decodes an address signal to output a signal of an amplitude of (Vpp-Vbb) specifying a word line in a word line group. A word driver provided corresponding to each word line transmits a word line specifying signal or a negative potential to the corresponding word line in accordance with signals WD and ZWD sent from a level converting circuit. The nonselected word line receives negative potential Vbb from a word driver. The selected word line receives high voltage Vpp from the word driver. It is possible to suppress a channel leak current at a memory transistor in the nonselected memory cell, which may be caused by the potential change of the word line and/or bit line, and a charge holding characteristic of the memory cell can be improved.

12 Claims, 43 Drawing Sheets